Dielectric Characterization of Bulk and Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt Thin Film Capacitors: Thickness Scaling and Interface Engineering for Energy Storage

Asmin M.K. [a,*], Smitha P.S. [a], V. Suresh Babu [b]

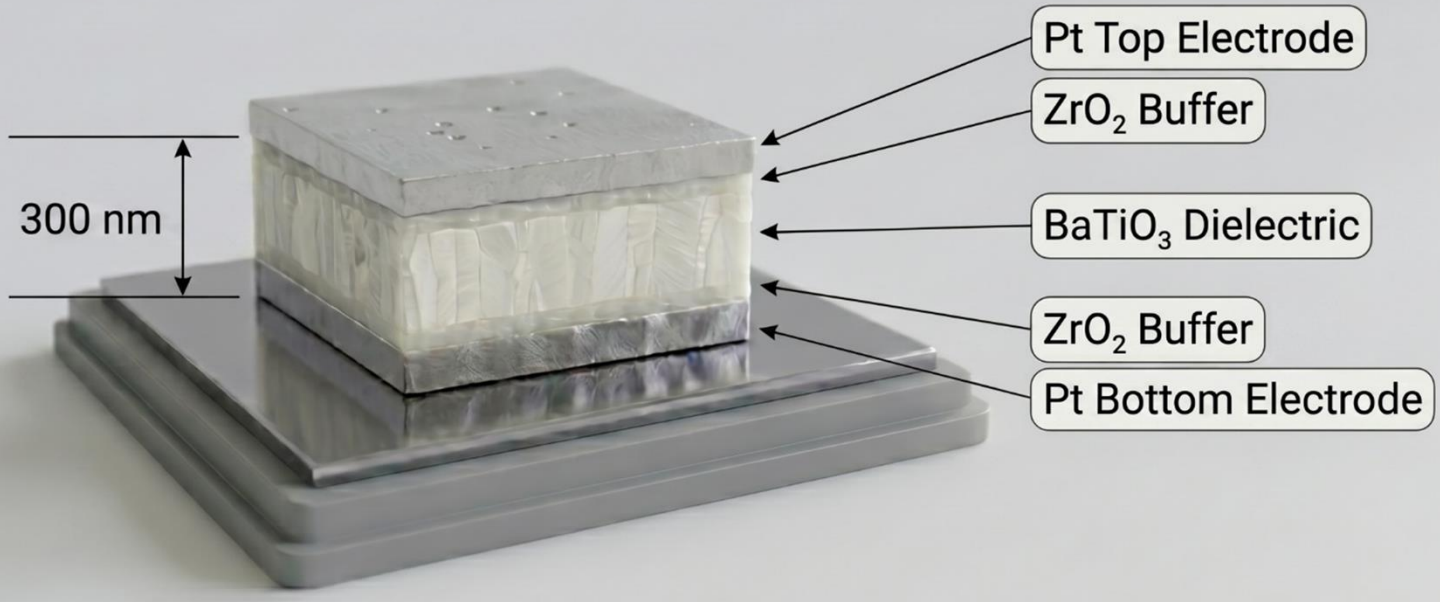
[a] *SCT College of Engineering, Trivandrum, Kerala 695018, India*

[b] *Mohandas College of Engineering and Technology, Trivandrum 695544, India*

Editor's note: Transitioning BZT-based capacitors, promising dielectric energy storage systems, to nanoscale thin films faces challenges such as increased leakage current. This study by Asmin M.K. et al. links bulk ceramic behavior with thin-film design through experiments and simulations. Their results confirm that although thinner Ag/BZT/Ag capacitors enhance capacitance and energy density, they also increase leakage current. Incorporating ZrO_2 barriers and high-Schottky-barrier Pt electrodes helps reduce leakage but lowers capacitance density.

doi: 10.22034/jams.2026.260305

How to cite: A. M.K. et al., *Journal of Applied Material Science*, **2026**, *2*, 260305.



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Journal of Applied Material Science **2026**, 2, 260305
How to cite: A. M.K. et al., *Journal of Applied Material Science*, **2026**, 2, 260305.
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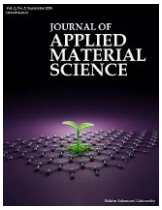

Original Research

Dielectric Characterization of Bulk and Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt Thin Film Capacitors: Thickness Scaling and Interface Engineering for Energy Storage

Asmin M.K. [a,*], Smitha P.S. [a], V. Suresh Babu [b]

[a] *SCT College of Engineering, Trivandrum, Kerala 695018, India*

[b] *Mohandas College of Engineering and Technology, Trivandrum 695544, India*

Abstract

$Ba(Zr_{0.2}Ti_{0.8})O_3$ (BZT) based capacitors are promising candidates for dielectric energy storage; however, the transition from bulk ceramics to nanoscale thin film devices is often limited by increased leakage current and reduced reliability. In this work, a systematic investigation is carried out to bridge bulk ceramic behavior and thin-film capacitor design through a combined experimental and simulation-based approach. Ag/BZT/Ag bulk ceramic capacitors were fabricated using the conventional solid-state reaction method and experimentally characterized. Thickness scaling effects were then analyzed by simulating an Ag/BZT/Ag capacitor with the dielectric thickness reduced to 104 nm while preserving the same lateral dimensions. Furthermore, a Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt thin-film capacitor architecture incorporating ZrO_2 interfacial barrier layers was modeled to suppress leakage current. The results demonstrate that thickness scaling significantly enhances capacitance and energy density but leads to a pronounced increase in leakage current density due to intensified electric fields and charge injection. The introduction of ZrO_2 barrier layers and high-Schottky-barrier Pt electrodes effectively suppresses leakage current and dielectric loss, at the cost of reduced capacitance density due to series capacitance effects. This study provides a comprehensive framework linking bulk ceramic performance, thickness scaling limitations, and interface-engineered thin-film design, offering valuable guidelines for the development of high-performance dielectric energy storage capacitors.

Keywords: Ceramic capacitor; Capacitance density; Thin film capacitor; Leakage current.

1. Introduction

The growing demand for compact, efficient, and reliable energy storage systems has intensified research on dielectric capacitors for applications requiring high power density, rapid charge capability, and long-term cycling stability. Among various dielectric materials, $BaTiO_3$-based ceramics have attracted considerable

* Corresponding author.
Email address: asmin@sctce.ac.in (A. M.K.)

Received 17 February 2026
Revised 10 June 2026
Accepted 26 June 2026
Available online 26 August 2026

https://doi.org/10.22034/jams.2026.260305

attention owing to their high dielectric permittivity, ferroelectric behavior, and chemical stability, making them promising candidates for energy storage applications [1-3]. However, pure $BaTiO_3$ exhibits temperature-dependent dielectric properties, relatively high dielectric loss, and increased leakage current under high electric fields, which limit its practical applicability, particularly in miniaturized and thin-film devices [4].

To overcome these limitations, compositional modification of $BaTiO_3$ through aliovalent or isovalent substitution has been widely investigated. Among various approaches, Zr substitution at the Ti site to form $BaTi_{1-x}Zr_xO_3$ (BZT) has been reported to improve dielectric stability, broaden the phase transition, and enhance energy-storage performance by reducing polarization hysteresis and dielectric loss [5-7]. The substitution of larger Zr^{4+} ions for Ti^{4+} induces lattice distortion and relaxor-like behavior, resulting in improved dielectric properties and breakdown strength. Consequently, BZT ceramics have demonstrated enhanced dielectric constant, lower dielectric loss, and improved energy storage density compared with pure $BaTiO_3$. Reported energy densities for bulk BZT and BCZT-based ceramics typically range from 0.3 to 3.5 J cm^{-3}, depending on composition and processing conditions [8-11].

With the increasing demand for device miniaturization and on-chip energy storage systems, extending high-permittivity BZT materials from bulk ceramics to thin-film capacitors has become an important research direction. Thin-film dielectric capacitors offer high volumetric efficiency and compatibility with integrated electronic systems [12]. Furthermore, nanoscale thickness reduction can significantly increase capacitance density and energy-storage capability. Thin-film ferroelectric and relaxor-ferroelectric capacitors have been reported to achieve energy densities in the range of 20–60 J cm^{-3} under high electric fields [12, 13]. However, dielectric thickness scaling introduces several challenges, including enhanced electric field intensity, increased charge injection from electrodes, and activation of field-assisted conduction mechanisms.

In particular, Schottky emission and Poole-Frenkel conduction become increasingly significant in thin dielectric layers. Schottky emission involves thermally assisted carrier injection from the electrode into the dielectric under an applied electric field, whereas Poole-Frenkel conduction arises from field-enhanced release of trapped charge carriers from defect states within the dielectric. These mechanisms, together with tunnelling-assisted transport, contribute to increased leakage current, reduced energy storage efficiency and degraded device reliability in nanoscale capacitors [14].

To address leakage current and breakdown-related limitations, interface engineering using dielectric barrier layers has emerged as an effective strategy. Multilayer and sandwich-structured capacitors incorporating insulating oxide layers have demonstrated improved dielectric strength and enhanced energy-storage performance [15]. Among various candidates, ZrO_2 is particularly attractive because of its wide bandgap, high dielectric strength, excellent thermal stability, and compatibility with $BaTiO_3$-based systems [16, 17]. The incorporation of ultrathin ZrO_2 interfacial layers at the electrode dielectric interface can suppress charge injection, improve electric field distribution, reduce oxygen vacancy migration, and thereby significantly lower leakage current while enhancing device reliability.

Recent simulation-based investigations have further highlighted the importance of combining material modification, thickness optimization, and interface engineering for the design of advanced dielectric capacitors [18]. Although extensive studies have been conducted on BZT ceramics and barrier layer-engineered thin film capacitors individually, a systematic framework linking bulk ceramic behavior, thickness scaling effects, and interface-engineered thin film design remains limited in the literature.

Therefore, the novelty of the present work lies in establishing a unified correlation between experimentally characterized bulk BZT ceramic capacitors, thickness-scaled nanoscale capacitor models, and interface-engineered $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin-film capacitor architectures. First, Ag/BZT/Ag bulk ceramic capacitors are fabricated and experimentally characterized to establish baseline dielectric and energy storage properties. Subsequently, thickness scaling effects are investigated through COMSOL simulations by reducing the BZT dielectric layer to 104 nm while preserving the lateral dimensions of the ceramic capacitor. Finally, a $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ multilayer thin film capacitor incorporating 2 nm ZrO_2 interfacial barrier layers is analyzed to evaluate leakage current suppression and dielectric-performance trade-offs. By integrating

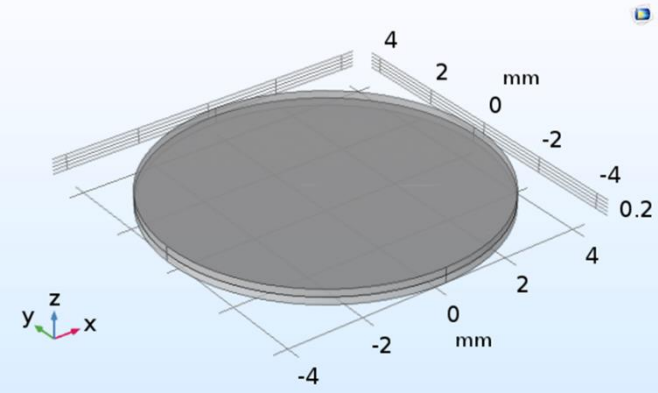

Figure 1. COMSOL simulation geometry of the thickness-scaled Ag/BZT/Ag capacitor (104 nm BZT layer).

experimental characterization with simulation-based analysis, this study provides insight into the transition from bulk ceramic capacitors to interface-engineered thin film energy storage devices and offers practical design guidelines for next-generation dielectric capacitors.

2. Experimental

2.1. Fabrication of Ag/BZT/Ag ceramic capacitor

$Ba(Zr_{0.2}Ti_{0.8})O_3$ (BZT) ceramic was synthesized using the conventional solid-state reaction method. High-purity $BaCO_3$ (99.9%), TiO_2 (99.9%), and ZrO_2 (99.9%) powders were used as starting materials and weighed according to the stoichiometric composition corresponding to x = 0.2. The powders were thoroughly mixed and ground in an agate mortar using ethanol as a dispersing medium to ensure homogeneous mixing. The resulting slurry was dried at 80 °C and subsequently ground into a fine powder.

The dried powder mixture was calcined at 1000 °C for 4 h in ambient air using a heating rate of 5 °C min^{-1} to promote phase formation. After calcination, the powder was reground manually to improve particle uniformity and reduce agglomeration. The resulting powder was uniaxially pressed into circular pellets with a radius of 4.37 mm using a hydraulic press.

The green pellets were sintered at 1350 °C for 4 h in ambient air with heating and cooling rates of 5 °C min^{-1} to obtain dense ceramic microstructures. Following sintering, both pellet surfaces were polished using fine abrasive paper to achieve uniform thickness and smooth electrode contact.

Silver paste was applied to both surfaces of the pellets to form Ag/BZT/Ag parallel plate capacitors for electrical characterization. The fabricated capacitors were used as bulk reference devices for dielectric, energy storage, and leakage current characterization.

2.2. Simulation of thickness-scaled ceramic and barrier layer thin film capacitors

Finite element simulations were performed using COMSOL Multiphysics to investigate the effects of thickness scaling and interface engineering on capacitor performance. Initially, the experimentally fabricated Ag/BZT/Ag ceramic capacitor was modeled by reducing the BZT dielectric thickness to 104 nm while maintaining the same lateral radius (4.37 mm) as the bulk ceramic capacitor, enabling direct comparison between bulk and nanoscale configurations. The three-dimensional simulation geometry of the thickness-scaled Ag/BZT/Ag capacitor is shown in Figure 1. The dielectric layer was assumed to be homogeneous, isotropic, and defect-free to isolate intrinsic electric-field-driven behavior. It should be noted that real dielectric materials contain grain boundaries, porosity, oxygen vacancies, and interface defects; therefore, the simulated results represent an idealized performance limit.

Subsequently, a multilayer $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin-film capacitor architecture was simulated, consisting of a 100 nm $BaTiO_3$ [16, 17] dielectric layer sandwiched between two 2 nm [16, 17] ZrO_2 interfacial barrier layers and platinum electrodes, as illustrated in Figures 2 and 3. The 104 nm dielectric thickness was

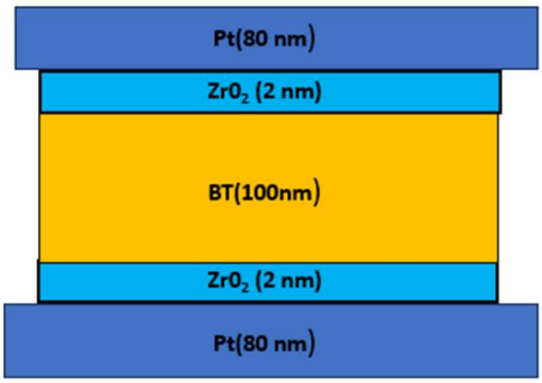

Figure 2. Schematic diagram of the $Pt/ZrO_2/BT/ZrO_2/Pt$ thin-film capacitor with interfacial barrier layers.

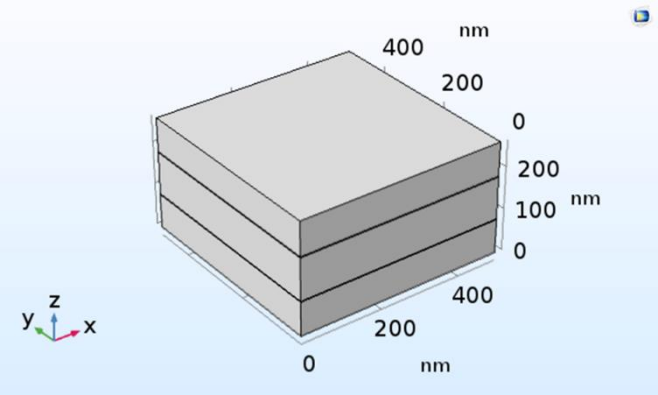

Figure 3. Simulated geometry of the Pt/ZrO_2/BT/ZrO_2/Pt thin-film capacitor with interfacial barrier layers.

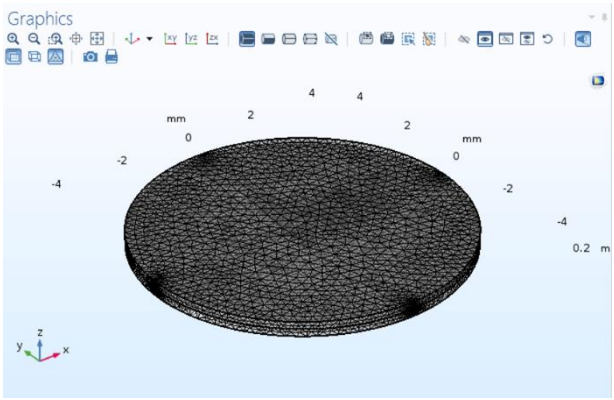

Figure 4. Physics-controlled normal tetrahedral mesh employed for the thickness-scaled Ag/BZT/Ag capacitor model with a 104 nm BZT dielectric layer.

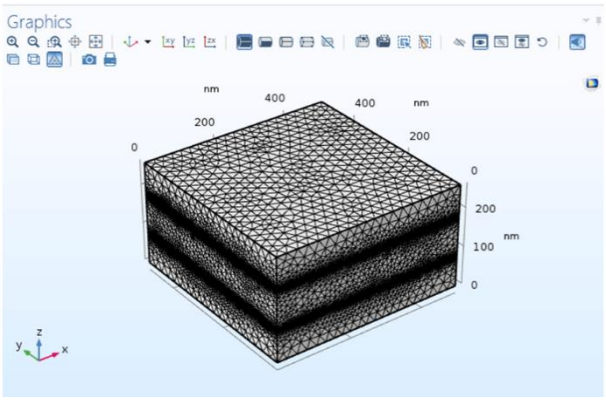

Figure 5. Physics-controlled finer tetrahedral mesh of the Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt thin film capacitor with refined interface regions and simulation accuracy.

selected to represent a typical nanoscale dielectric layer used in thin-film energy storage capacitors, while the 2 nm ZrO_2 layers were chosen based on reported barrier layer designs that effectively suppress charge injection without excessively reducing capacitance.

The Electrostatics and Electric Currents modules of COMSOL Multiphysics were employed for the simulations. A physics-controlled tetrahedral mesh was used for all models. The thickness-scaled Ag/BZT/Ag capacitor was discretized using a normal mesh, as shown in Figure 4, which provided sufficient accuracy for the relatively simple single-layer dielectric structure. In contrast, the Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt multilayer thin film capacitor was analyzed using a finer mesh, as shown in Figure 5, to accurately resolve the ultrathin 2 nm ZrO_2 interfacial layers and capture the strong electric field gradients occurring at the dielectric interfaces. The mesh refinement ensured improved numerical accuracy in evaluating capacitance density, dielectric loss, energy density, electric field distribution, and leakage current density.

The ZrO_2 barrier layers were incorporated to suppress charge injection, reduce oxygen-vacancy migration, and improve electric field distribution within the dielectric stack, whereas Pt electrodes were selected to represent high Schottky barrier contacts. Electric field-dependent conduction models were employed to analyze leakage-current behavior, including field-assisted carrier transport mechanisms relevant to nanoscale dielectric structures.

The simulations were used to evaluate capacitance density, dielectric loss, energy density, electric-field distribution, and leakage current density. This simulation methodology provides insight into the transition from bulk ceramic behavior to interface-engineered thin-film capacitor design and helps establish design guidelines for high-performance dielectric energy-storage capacitors.

To evaluate the robustness of the simulation results, dielectric permittivity values were varied by ±10%. Although the absolute values of capacitance density and energy density changed slightly, the overall trends regarding thickness scaling and leakage-current suppression remained unchanged, confirming the reliability of the conclusions.

2.3. *Measurements*

Dielectric measurements were performed using a Hioki IM3536 LCR meter over the frequency range of 10

Hz to 1 MHz at room temperature with an AC excitation voltage of 1 V. The capacitance and dielectric loss of the fabricated Ag/BZT/Ag capacitors were evaluated as a function of frequency. Leakage current measurements were carried out using a Keithley 2450 SourceMeter under DC bias voltages ranging from 0 to 10 V to investigate the conduction behavior and leakage characteristics of the capacitors.

3. Results and discussion

3.1. Capacitance density

Figure 6 presents the frequency-dependent capacitance density of three capacitor configurations: (i) experimentally fabricated Ag/BZT/Ag bulk ceramic capacitor, (ii) simulated Ag/BZT/Ag ceramic capacitor, and (iii) simulated Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt thin-film capacitor. Although all three systems are based on $BaTiO_3$-derived dielectrics, their electrical performance differs significantly due to variations in device geometry, thickness, and interface structure.

The Ag/BZT/Ag bulk ceramic capacitor exhibits the lowest capacitance density across the entire frequency range. This behavior is primarily attributed to the large thickness of the ceramic dielectric layer, which is on the order of millimeters. According to the parallel-plate capacitor relation $C/A = \varepsilon_0\varepsilon_r/t$, capacitance density is inversely proportional to dielectric thickness (t). Despite the high intrinsic dielectric constant of BZT ceramics, the large thickness severely limits the achievable capacitance density. Furthermore, bulk ceramics contain grain boundaries, pores, and microstructural inhomogeneities that contribute to interfacial polarization only at low frequencies, resulting in relatively frequency-stable but low capacitance density values [19-21].

The simulated Ag/BZT/Ag ceramic capacitor shows a substantially higher capacitance density compared to the experimentally measured ceramic. This increase arises not only from the idealized simulation conditions, where effects such as porosity, imperfect electrode contact, and microstructural defects are neglected, but also from the significant reduction in dielectric thickness to 104 nm in the simulated model.

In the simulations, the dielectric layer is assumed to be uniform, dense, and defect-free, allowing the intrinsic permittivity of BZT to dominate the response. Moreover, the drastic reduction in thickness enhances the capacitance density according to the inverse thickness dependence of parallel-plate capacitors. As a result, the simulated ceramic capacitor demonstrates enhanced capacitance density and reduced frequency dispersion relative to the experimental counterpart. This discrepancy between experimental and simulated results is commonly observed in ferroelectric ceramics and highlights the combined influence of thickness scaling and real microstructural constraints in limiting practical device performance [22, 23].

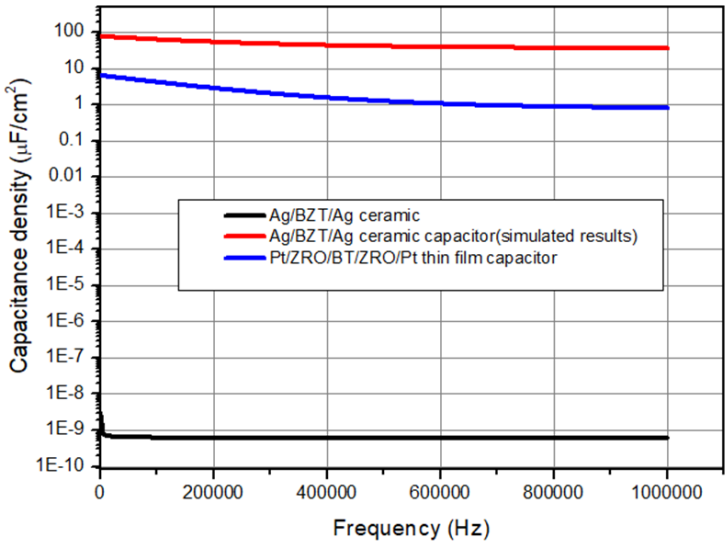

Figure 6. Capacitance density versus frequency for bulk BZT ceramic, scaled BZT ceramic (104 nm, simulated), and ZrO_2 barrier-layer-engineered thin-film capacitor.

The $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin-film capacitor exhibits a lower capacitance density compared to the simulated Ag/BZT/Ag ceramic capacitor with 104 nm thickness, despite offering improved leakage suppression. This reduction in capacitance density is primarily attributed to the introduction of ZrO_2 interfacial barrier layers, which possess a lower dielectric constant than BZT.

In a multilayer capacitor structure, the overall capacitance is governed by the series combination of individual dielectric layers, and the inclusion of low-permittivity ZrO_2 layers effectively reduces the net capacitance density of the device. Although the ZrO_2 layers decrease the effective dielectric constant, they play a critical role in suppressing charge injection from the electrodes and redistributing the internal electric field, thereby mitigating leakage current and enhancing dielectric reliability. This trade-off between capacitance density and leakage control is well documented in barrier layer-engineered dielectric capacitors and highlights the necessity of interface engineering to achieve stable energy storage performance in thin-film devices [24-26].

3.2. Dielectric loss

Figure 7 illustrates the variation of dielectric loss (tan δ) as a function of frequency for three capacitor configurations: the experimentally fabricated Ag/BZT/Ag bulk ceramic capacitor, the simulated Ag/BZT/Ag ceramic capacitor, and the simulated $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin-film capacitor. A pronounced difference in dielectric loss behavior is observed among the three systems, highlighting the combined influence of dielectric thickness, microstructural effects, and interfacial engineering.

The Ag/BZT/Ag bulk ceramic capacitor exhibits the highest dielectric loss across the measured frequency range. At low frequencies, the elevated loss can be attributed to space charge polarization, grain boundary contributions, and defect-assisted conduction mechanisms inherent to bulk ceramic materials.

As the frequency increases, the dielectric loss decreases gradually due to the reduced ability of charge carriers and dipoles to follow the alternating electric field, resulting in a more stable response at higher frequencies. This behavior is characteristic of polycrystalline ferroelectric ceramics and is widely reported in $BaTiO_3$-based systems.

In contrast, the simulated Ag/BZT/Ag ceramic capacitor shows a significantly lower and nearly frequency-independent dielectric loss. This reduction arises from the idealized simulation conditions, where the dielectric layer is assumed to be dense, uniform, and free from microstructural defects such as pores and grain boundaries. Moreover, the reduced dielectric thickness in the simulated configuration minimizes bulk

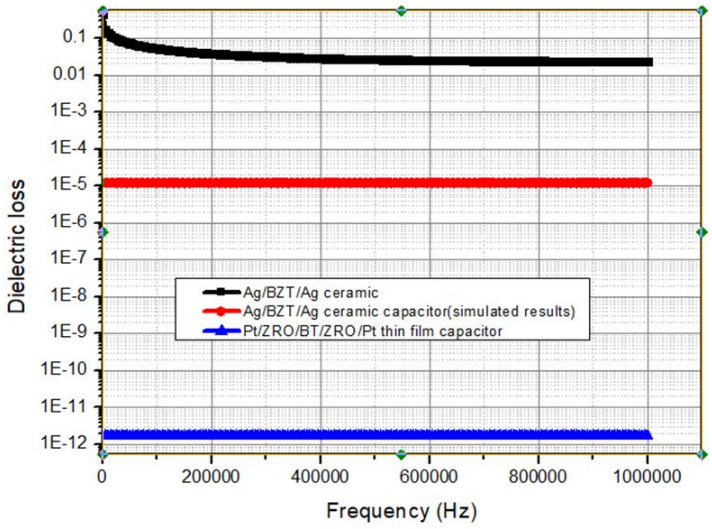

Figure 7. Dielectric loss versus frequency for bulk BZT ceramic, scaled BZT ceramic (104 nm, simulated), and ZrO_2 barrier-layer-engineered thin-film capacitor.

conduction paths and suppresses interfacial polarization losses, leading to an overall decrease in dielectric loss compared to the experimental ceramic.

The $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin film capacitor exhibits the lowest dielectric loss among all three configurations, remaining almost constant across the entire frequency range. This exceptional loss suppression is primarily attributed to the presence of ZrO_2 interfacial barrier layers, which possess a wide bandgap and high electrical resistivity. These barrier layers effectively block charge injection from the metal electrodes, reduce leakage-related losses, and homogenize the internal electric field distribution. Consequently, conduction-related loss mechanisms are strongly suppressed, resulting in superior dielectric stability.

Overall, the comparative analysis demonstrates that while bulk BZT ceramics suffer from higher dielectric loss due to microstructural and space-charge effects, thickness scaling and interface engineering significantly improve dielectric performance. In particular, the incorporation of ZrO_2 barrier layers in the thin-film capacitor architecture proves highly effective in minimizing dielectric loss, making this structure especially attractive for high-efficiency energy storage applications.

3.3. Energy density

The experimentally measured energy density of bulk BZT ceramic in this study was calculated from the stored electrostatic energy per unit volume using:

$$U = \frac{CV^2}{2Ad} \quad (1)$$

where (U) is the volumetric energy density (J/cm^3), (C) is the capacitance, (V) is the applied voltage, (A) is the electrode area, and (d) is the dielectric thickness. The calculated energy density of bulk BZT ceramic is 0.841 J/cm^3, which agrees well with reported values for bulk BZT- and BCZT-based ceramics (0.3–3.5 J/cm^3) that are limited by dielectric breakdown strength and ferroelectric domain losses in thick ceramic structures [10, 11]. For the simulated capacitor configurations, the energy density values were obtained directly from the electrostatic energy-density distributions calculated by COMSOL Multiphysics. COMSOL simulations show that reducing the dielectric thickness to 104 nm while maintaining the same lateral radius dramatically increases the energy density to approximately 45 J/cm^3, demonstrating the strong thickness-scaling effect on breakdown field and electric-field endurance in nanoscale dielectric films. The corresponding energy-density distribution map (Figure 8) exhibits a highly uniform and concentrated energy-storage region across the thin BZT layer, indicating effective electric-field confinement, suppressed domain wall motion, and enhanced polarization efficiency under high electric fields. This trend is consistent with reports of ultrahigh energy densities (30–60 J/cm^3) in thin-film relaxor ferroelectrics and lead-free thin films operating under megavolt-per-centimeter fields [13].

In contrast, the simulated $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ multilayer stack yields a reduced energy density of approximately 6 J/cm^3, as illustrated in the layer-

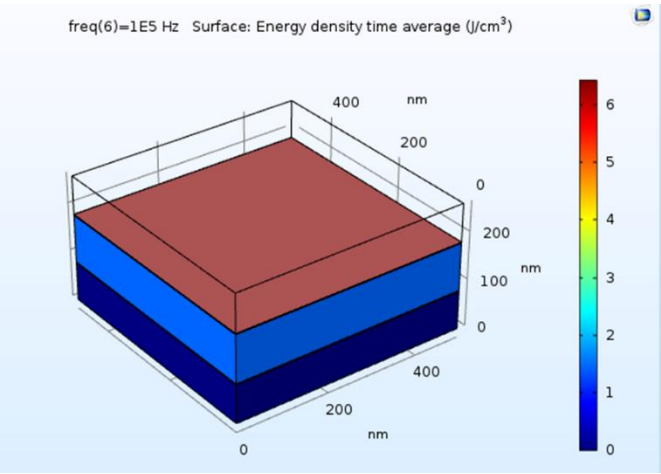

Figure 8. Energy density distribution in a BZT thin-film ceramic capacitor.

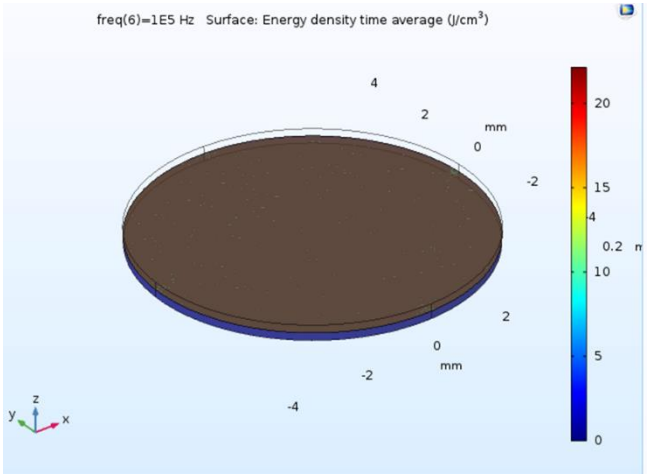

Figure 9. Energy density distribution in a $Pt/ZrO_2/BT/ZrO_2/Pt$ thin-film ceramic capacitor.

resolved energy-density contour plot (Figure 9), which reveals a nonuniform energy distribution across dielectric layers due to electric-field partitioning and dielectric mismatch. This reduction relative to the single-layer BZT thin film is attributed to series capacitance effects, interfacial polarization losses, electric-field screening at metal–oxide boundaries, and charge trapping at Pt/ZrO_2 and ZrO_2/$BaTiO_3$ interfaces, all of which reduce the effective recoverable energy density. Comparable energy-storage values (5–15 J/cm^3) have been reported in multilayer ceramic and oxide heterostructure capacitors, where interface-dominated polarization dynamics limit peak performance [27]. Overall, these results confirm that nanoscale thickness reduction significantly enhances intrinsic energy-storage capability, whereas multilayer heterostructuring introduces interfacial and dielectric coupling effects that moderate net energy density, revealing a trade-off between field endurance, interface stability, and maximum recoverable energy performance.

3.4. Leakage current density

Figure 10 illustrates the leakage current density characteristics of three capacitor configurations: a fabricated Ag/BZT/Ag ceramic capacitor, a simulated Ag/BZT/Ag ceramic structure with thickness reduced to 104 nm while maintaining the same electrode area, and a Pt/ZrO_2/BT/ZrO_2/Pt thin film capacitor incorporating interfacial barrier layers. The fabricated Ag/BZT/Ag ceramic capacitor exhibits moderate leakage current density, governed by bulk-limited conduction and interface-related defects typical of ceramic dielectrics. Upon reducing the thickness to 104 nm in the simulated Ag/BZT/Ag structure, a significant increase in leakage current density is observed, which is primarily attributed to the enhanced electric field (E = V/t) resulting from thickness scaling, thereby activating field-assisted conduction mechanisms such as Schottky emission and Poole-Frenkel transport. Furthermore, Ag electrodes form relatively low Schottky barriers with oxide dielectrics, facilitating carrier injection and further increasing leakage.

In contrast, the Pt/ZrO_2/BT/ZrO_2/Pt capacitor demonstrates a marked reduction in leakage current density despite its thin film nature, owing to the presence of ZrO_2 interfacial layers that act as effective leakage barriers by suppressing oxygen vacancy migration and limiting charge injection, along with the higher Schottky barrier height formed at Pt–dielectric interfaces. These results emphasize that while thickness scaling in ceramic capacitors leads to increased leakage current density, appropriate electrode selection and interface engineering can effectively suppress leakage in thin-film ferroelectric capacitors [28-31].

3.5. Comparison with related works

The energy density obtained for bulk BZT ceramic in this study (≈ 0.84 J cm^{-3}) is consistent with previously

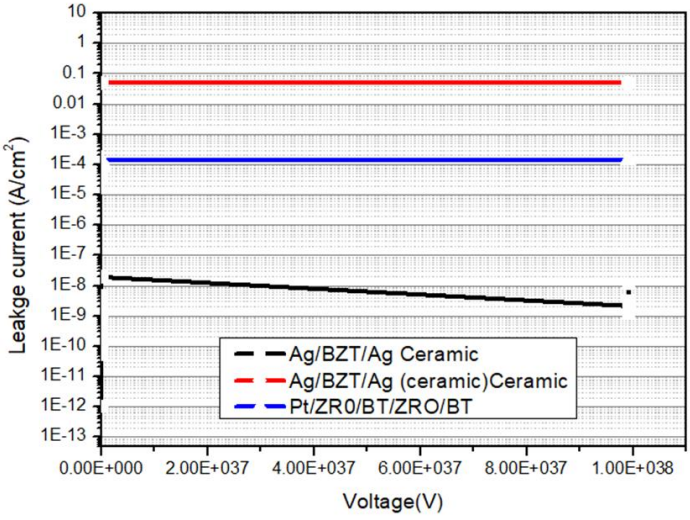

Figure 10. LCD versus voltage for bulk BZT ceramic, scaled BZT ceramic (104 nm, simulated), and ZrO_2 barrier-layer-engineered thin-film capacitor.

Table 1. Comparative summary of dielectric and energy-storage performance of bulk, thickness-scaled, and interface-engineered BZT-based capacitors

Material / Structure	Form	Dielectric Thickness	Energy Density (J/cm³)	Leakage Current Density (A/cm²)	Key Strategy	Reference
$BaTiO_3$ ceramic	Bulk	mm-scale	0.2–1.0	10^{-8}–10^{-7}	Conventional ceramic	[1, 2]
BCZT ceramic	Bulk	mm-scale	0.3–3.5	10^{-8}–10^{-6}	Compositional modification	[10, 11]
BZT ceramic (x ≈ 0.2–0.3)	Bulk	mm-scale	0.5–2.5	10^{-8}–10^{-9}	Zr substitution	[8, 9]
Ag/BZT/Ag (this work)	Bulk ceramic	mm-scale	0.84	10^{-8}–10^{-9}	Experimental ceramic	This work
$BaTiO_3$ thin film	Thin film	100–300 nm	20–40	10^{-4}–10^{-3}	Thickness scaling	[12, 14]
Relaxor ferroelectric thin film	Thin film	100–500 nm	30–60	10^{-4}–10^{-2}	High-field operation	[13]
Ag/BZT/Ag (this work)	Thickness-scaled (simulated)	104 nm	~45	~10^{-2}	Thickness scaling	This work
Multilayer oxide capacitor	Thin film	100–300 nm	5–15	10^{-6}–10^{-5}	Barrier-layer engineering	[27]
ZrO_2-barrier ferroelectric film	Thin film	100–200 nm	5–12	10^{-6}–10^{-4}	Interface engineering	[16, 17]
Pt/ZrO_2/BT/ZrO_2/Pt (this work)	Thin film (simulated)	100 nm BT + 2 nm ZrO_2	~6	~10^{-4}	Barrier layers + Pt electrodes	This work

reported values for BZT- and BCZT-based ceramics, which typically lie in the range of 0.3–3.5 J cm^{-3} and are primarily constrained by dielectric breakdown strength and ferroelectric domain-related losses inherent to thick ceramic structures [10, 11]. Upon thickness scaling to the nanoscale, the simulated BZT capacitor achieves a significantly enhanced energy density of approximately 45 J cm^{-3}, falling well within the range reported for thin-film relaxor ferroelectrics and lead-free dielectric films operating under high electric fields (30–60 J cm^{-3}) [13]. However, in agreement with earlier reports on $BaTiO_3$- and BZT-based thin films, this improvement is accompanied by an increase in leakage current density due to intensified electric fields and field-assisted conduction mechanisms such as Schottky emission and Poole–Frenkel transport [12, 14].

Compared with previously reported multilayer and sandwich structured dielectric capacitors [15, 16, 27], the Pt/ZrO_2/$BaTiO_3$/ZrO_2/Pt architecture investigated in this work demonstrates effective leakage current suppression and reduced dielectric loss, confirming the role of ZrO_2 interfacial layers as efficient charge blocking barriers. The resulting energy density (~6 J cm^{-3}) is comparable to values reported for oxide-based multilayer thin film capacitors, where interface-dominated polarization behavior and series capacitance effects limit the maximum recoverable energy density [27-31]. Table 1 summarizes and compares the energy density, leakage current density, and design strategies of the present work with representative bulk, thickness scaled, and interface engineered dielectric capacitors reported in the literature, highlighting the trade-off between thickness scaling induced energy density enhancement and interface engineering driven leakage suppression. Unlike many prior studies that focus exclusively on thin film architectures, the present work establishes a unified correlation between bulk ceramic behavior, nanoscale thickness scaling, and barrier-layer-engineered thin-film performance, offering comprehensive insight into the design trade-offs governing next-generation dielectric energy storage capacitors.

4. Conclusions

In summary, this work presents a comprehensive investigation of BZT-based capacitors spanning bulk ceramic, thickness-scaled ceramic, and barrier layer-engineered thin-film architectures. Experimental results confirm that bulk Ag/BZT/Ag ceramic capacitors

exhibit stable dielectric behavior with low leakage current density but limited capacitance and energy density due to their large thickness. Simulation results reveal that reducing the BZT dielectric thickness to 104 nm dramatically enhances capacitance density and energy storage capability; however, this improvement is accompanied by a substantial increase in leakage current density arising from enhanced electric fields and field-assisted conduction mechanisms. By introducing ZrO_2 interfacial barrier layers and Pt electrodes in a $Pt/ZrO_2/BaTiO_3/ZrO_2/Pt$ thin-film configuration, leakage current and dielectric loss are significantly suppressed through reduced charge injection and improved electric-field distribution, albeit with a moderate reduction in effective capacitance and energy density due to series dielectric effects. These findings highlight the critical trade-off between energy density enhancement and leakage control and underscore the importance of interface engineering in enabling reliable thin-film dielectric capacitors. The combined experimental simulation approach adopted in this study offers a robust pathway for translating bulk ferroelectric ceramics into practical thin-film energy storage devices.

Conflict of Interest

The authors declare no conflict of interest.

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